

WHAT IS CLAIMED IS:

1. A processor comprising:

5 a register file including at least a first register and a second register; and

an execution core coupled to the register file and coupled to receive an instruction including a register address field having a first encoding, wherein, dependent on a first field of the instruction, the execution core is

10 configured to select which of a first portion of the first register and a second portion of the second register is used as an operand of the instruction responsive to the first encoding of the register address field.

2. The processor as recited in claim 1 wherein the first field is a prefix field, and wherein

15 the execution core is configured to select the first portion of the first register in response to a presence of the prefix field in the instruction, and wherein the execution core is configured to select the second portion of the second register in response to an absence of the prefix field in the instruction.

20 3. The processor as recited in claim 2 wherein the prefix field is a prefix byte.

4. The processor as recited in claim 1 wherein the first portion is a first byte and the second portion is a second byte.

25 5. The processor as recited in claim 4 wherein the first byte is a least significant byte of the first register and wherein the second byte is a next to least significant byte of the second register.

6. An apparatus comprising:

one or more storage locations corresponding to at least a first register and a second register; and

5 a processor coupled to the one or more storage locations and coupled to receive an instruction including a register address field having a first encoding, wherein, dependent on a first field of the instruction, the processor is configured to select which of a first portion of the first register and a second portion of the second register is used as an operand of the
10 instruction responsive to the first encoding of the register address field.

7. The apparatus as recited in claim 1 wherein the first field is a prefix field, and wherein the processor is configured to select the first portion of the first register in response to a presence of the prefix field in the instruction, and wherein the processor is configured to
15 select the second portion of the second register in response to an absence of the prefix field in the instruction.

8. The apparatus as recited in claim 7 wherein the prefix field is a prefix byte.

20 9. The apparatus as recited in claim 6 wherein the first portion is a first byte and the second portion is a second byte.

10. The apparatus as recited in claim 9 wherein the first byte is a least significant byte of the first register and wherein the second byte is a next to least significant byte of the
25 second register.

11. A method comprising:

receiving an instruction including a register address field having a first encoding;

and

5 selecting which of a first portion of a first register and a second portion of a second register is used as an operand of the instruction responsive to the first encoding, the selecting dependent on a first field of the instruction.

12. The method as recited in claim 11 wherein the first field is a prefix field, and wherein the selecting comprises:

10 selecting the first portion of the first register in response to a presence of the prefix field in the instruction; and

selecting the second portion of the second register in response to an absence of the prefix field in the instruction.

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13. The method as recited in claim 12 wherein the prefix field is a prefix byte.

14. The method as recited in claim 11 wherein the first portion is a first byte and the second portion is a second byte.

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15. The method as recited in claim 14 wherein the first byte is a least significant byte of the first register and wherein the second byte is a next to least significant byte of the second register.

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16. A processor comprising:

a register file including a plurality of registers; and

an execution core coupled to the register file, wherein the execution core is

configured, dependent on a first field of an instruction also having a register address field, to: (i) select a first portion of one of the plurality of registers as an operand of the instruction, the one of the plurality of registers selected responsive to a value of the register address field; or (ii) select one of a first portion or a second portion of one of a subset of the plurality of registers as the operand of the instruction, the first portion or the second portion and the one of the subset selected responsive to a value of the register address field.

10 17. The processor as recited in claim 16 wherein the first field is a prefix field, and wherein the execution core is configured to select the first portion of the one of the plurality of registers in response to a presence of the prefix field in the instruction, and wherein the execution core is configured to select the first portion or the second portion of the one of the subset in response to an absence of the prefix field in the instruction.

15 18. The processor as recited in claim 17 wherein the prefix field is a prefix byte.

19. The processor as recited in claim 16 wherein the first portion is a first byte and the second portion is a second byte.

20 20. The processor as recited in claim 19 wherein the first byte is a least significant byte of a corresponding one of the plurality of registers and wherein the second byte is a next to least significant byte of the corresponding one of the plurality of registers.

25 21. An apparatus comprising:

one or more storage locations corresponding to a plurality of registers; and

a processor coupled to the one or more storage locations, wherein the processor is

configured, dependent on a first field of an instruction also having a register address field, to: (i) select a first portion of one of the plurality of registers as an operand of the instruction, the one of the plurality of registers selected responsive to a value of the register address field; or (ii) select one of a first portion or a second portion of one of a subset of the plurality of registers as the operand of the instruction, the first portion or the second portion and the one of the subset selected responsive to a value of the register address field.

22. The apparatus as recited in claim 21 wherein the first field is a prefix field, and wherein the processor is configured to select the first portion of the one of the plurality of registers in response to a presence of the prefix field in the instruction, and wherein the processor is configured to select the first portion or the second portion of the one of the subset in response to an absence of the prefix field in the instruction.

23. The apparatus as recited in claim 22 wherein the prefix field is a prefix byte.

24. The apparatus as recited in claim 21 wherein the first portion is a first byte and the second portion is a second byte.

25. The apparatus as recited in claim 24 wherein the first byte is a least significant byte of a corresponding one of the plurality of registers and wherein the second byte is a next to least significant byte of the corresponding one of the plurality of registers.

26. A method comprising:

(a) mapping each value of a register address field of an instruction to a first portion of a different one of the plurality of registers; or

(b) mapping each value of the register address field to a first portion or a second portion of different ones of a plurality of the plurality of registers;

wherein (a) or (b) is performed dependent on a first field of the instruction.

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27. The method as recited in claim 26 wherein the first field is a prefix field, and wherein (a) is performed in response to a presence of the prefix field in the instruction, and wherein (b) is performed in response to an absence of the prefix field in the instruction.

10 28. The method as recited in claim 27 wherein the prefix field is a prefix byte.

29. The method as recited in claim 26 wherein the first portion is a first byte and the second portion is a second byte.

15 30. The method as recited in claim 29 wherein the first byte is a least significant byte of a corresponding one of the plurality of registers and wherein the second byte is a next to least significant byte of the corresponding one of the plurality of registers.